ThalesAlenia Space
A Thales / Finmeccanica Company

Hervé ZUGAJ, Bernard BOULANGER

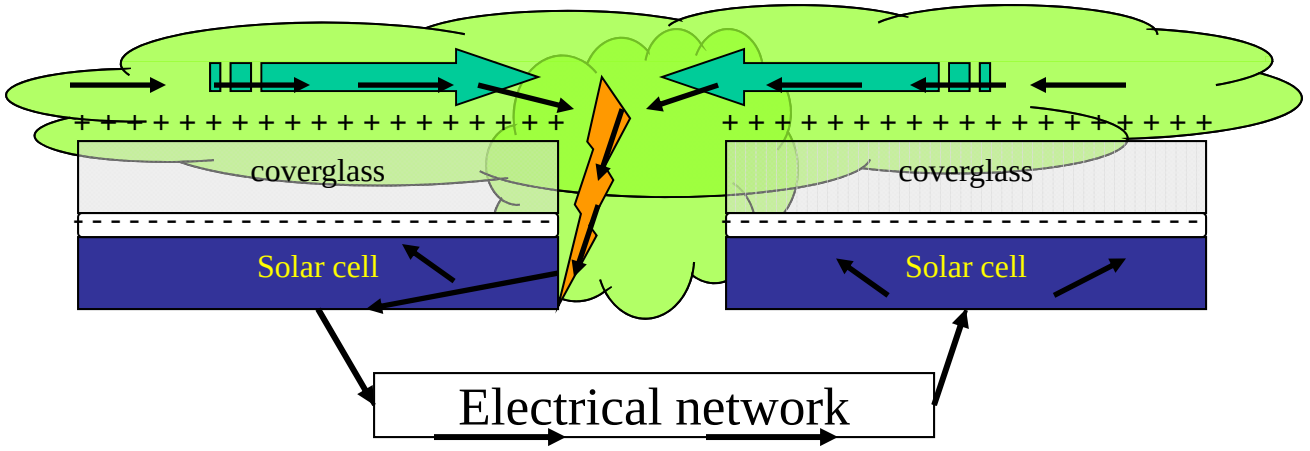
Solar array electrical architecture trade-off with GaAs cell protection against flashover current

Template reference : 100181670S-EN

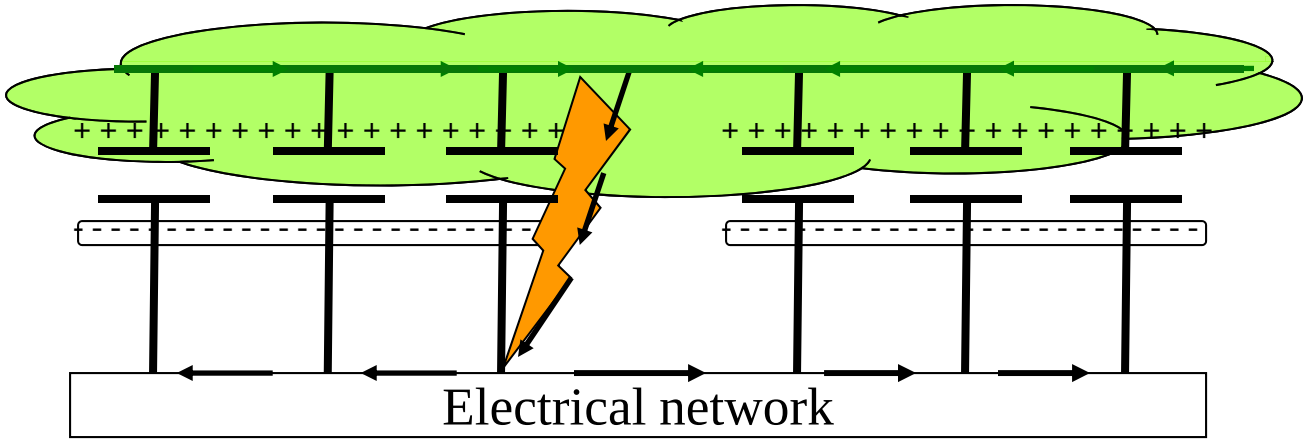
THALES

Coverglass discharge circuit

Coverglass electrostaticly charged in inverted voltage gradient mode

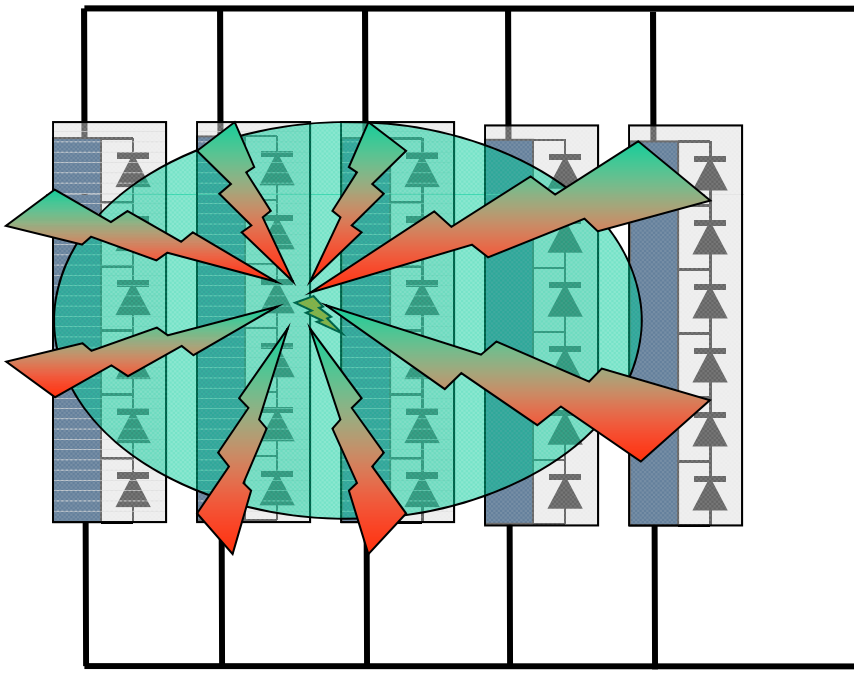


Equivalent coverglass discharge circuit



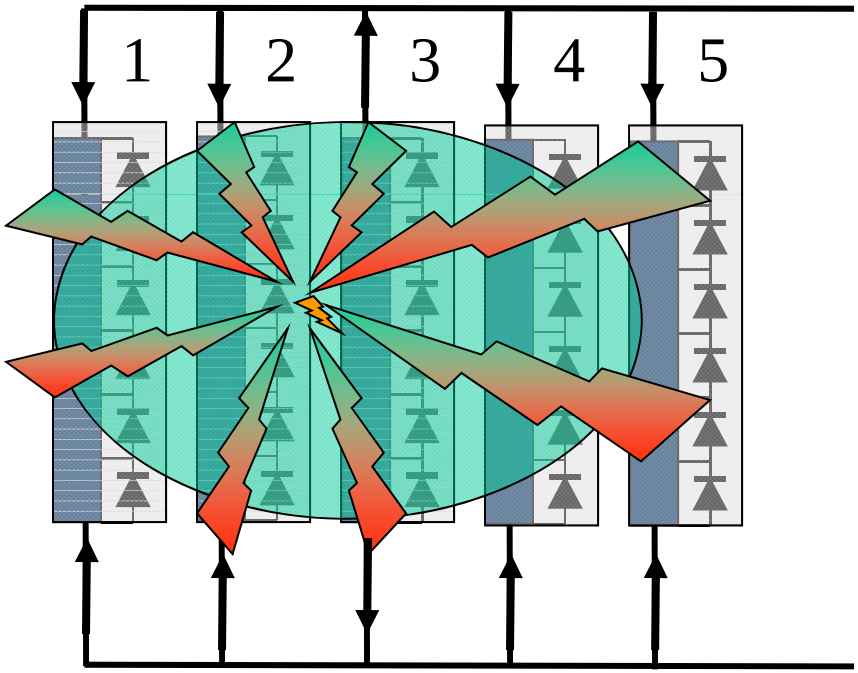
ESD in the gap between cells

5 circuits of GaAs cells with coverglasses and bypass diodes



Full Plasma propagation on the solar array panel

Currents between circuits



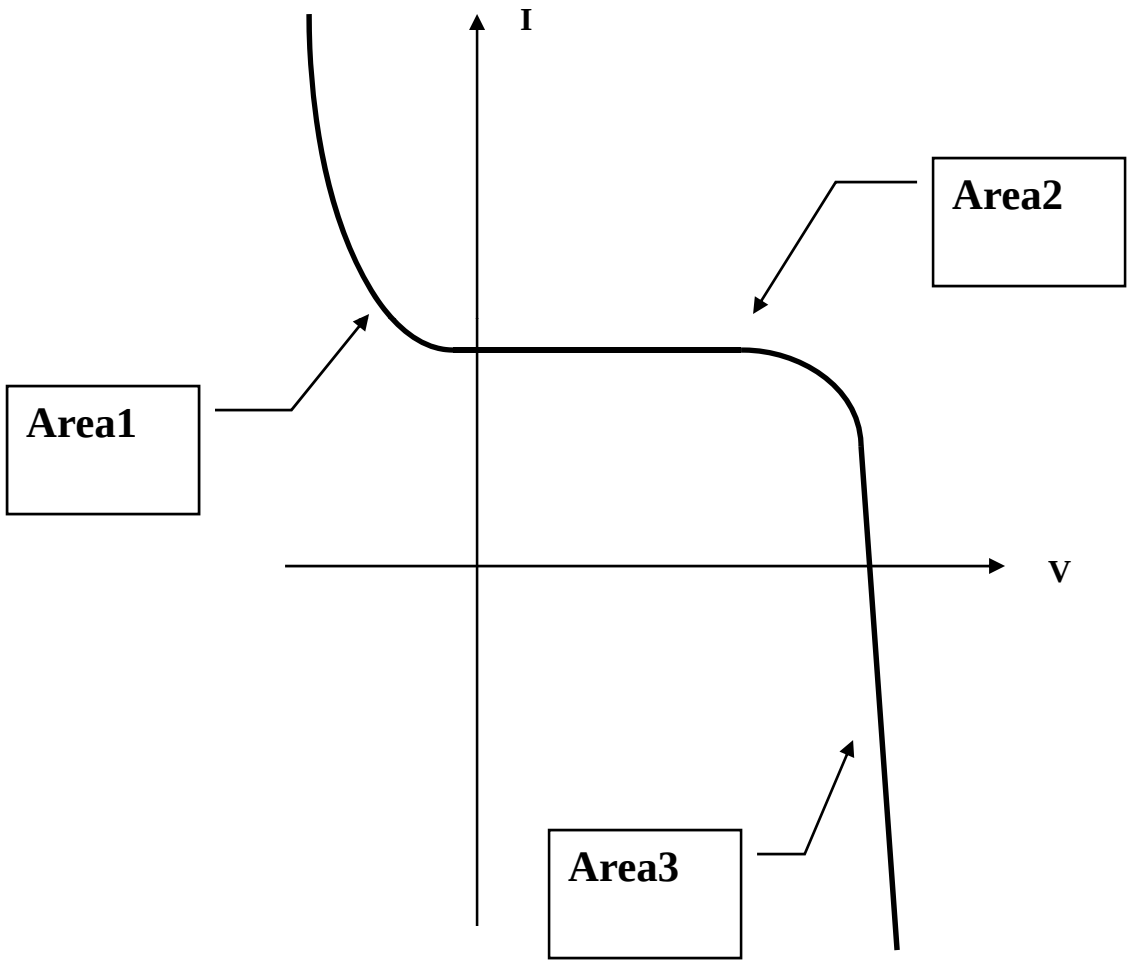
ESD site circuit current (n°3) is flowing outside.

Other discharged circuit currents (n°1-2-4-5) are flowing inside.

I/V curve of GaAs cell equipped with bypass diode

V is cell voltage =
Bypass diode reverse voltage,

I = forward cell current +
forward bypass diode current,



Cell reverse voltage case (Area 1)

Area 1 is the case of cequiteverse voltage which is equivalent to bypass diode forward mode.

In order to protect the GaAs cell against reverse voltage, in steady state and in case of ESD, bypass diode is commonly used in parallel to the solar cell. This protection is useful in case of cell shadowing.

Cell reverse current case (Area 3)

Area 3 is the case of cell reverse current, in this case the bypass diode is blocked in voltage reverse mode.

In steady state (no ESD), the cell reverse current is avoided in the commonly solar array architectures by using at least 1 blocking diode per solar cell circuit. This protection is useful in case of insulation failure.

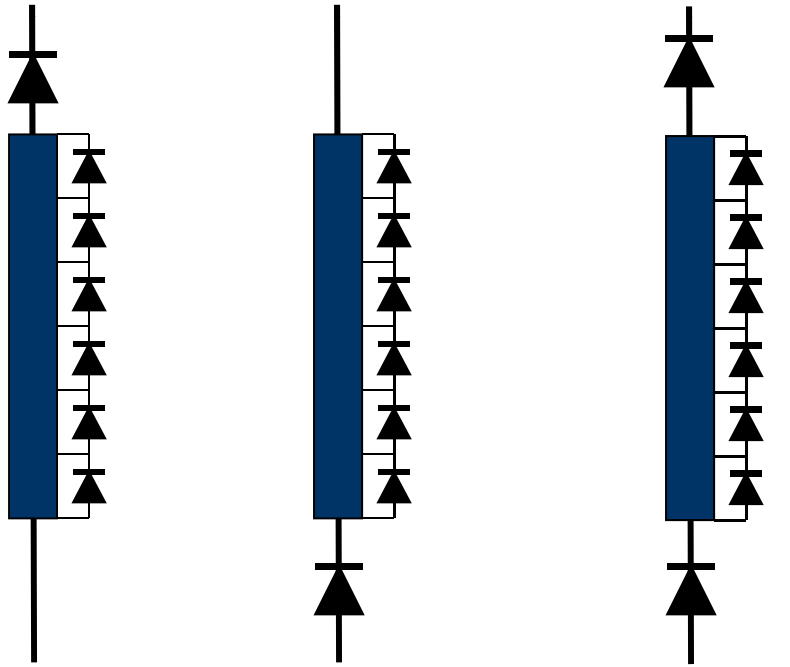
In case of ESD, cell reverse current pulse may degrade the GaAs cell if the pulse current and duration are enough high.

GaAs solar cell circuit architecture principles

Architectures commonly used on spacecraft,

The question is, are some GaAs cell in reverse current mode during ESD ?

Arch. 1 Arch. 2 Arch. 3



Bypass diode

Bypass diode may be sensitive to pulse current versus diode size and technology.

During ESD on solar panel, the bypass diode can be

- In reverse voltage mode, areas 2&3 ; this reverse voltage is generated
  - Area2, in steady state, by the protected GaAs cell, so the maximum diode reverse voltage is in the range 2.5V-5V.
  - Area 3,in case of ESD, by the protected GaAs cell voltage drop due to the ESD current. The estimation of this maximum voltage drop is in the range of 10-15V, assuming ESD current about 10A.

the bypass diode is robust if the diode voltage breakdown is about 50V

- in forward voltage mode,area1, the bypass diode may be sensitive to pulse current. The driving parameter is the active surface of the diode, so larger is the diode, more robust is the diode with regard to pulse current due to diode density current. We assume the diode performance is at least 25A repetitive surge current.

ESD site location

The ESD site location on the wing is driven by the coverglass electrostatic charge which is not constant on all the wing.

The ESD site location is quite randomly distributed on each panel in orbit, assuming the coverglass electrostatic charge difference on each panel is not enough large.

The question is How does this flashover current flow in the real solar array electrical network architecture versus ESD site location ?

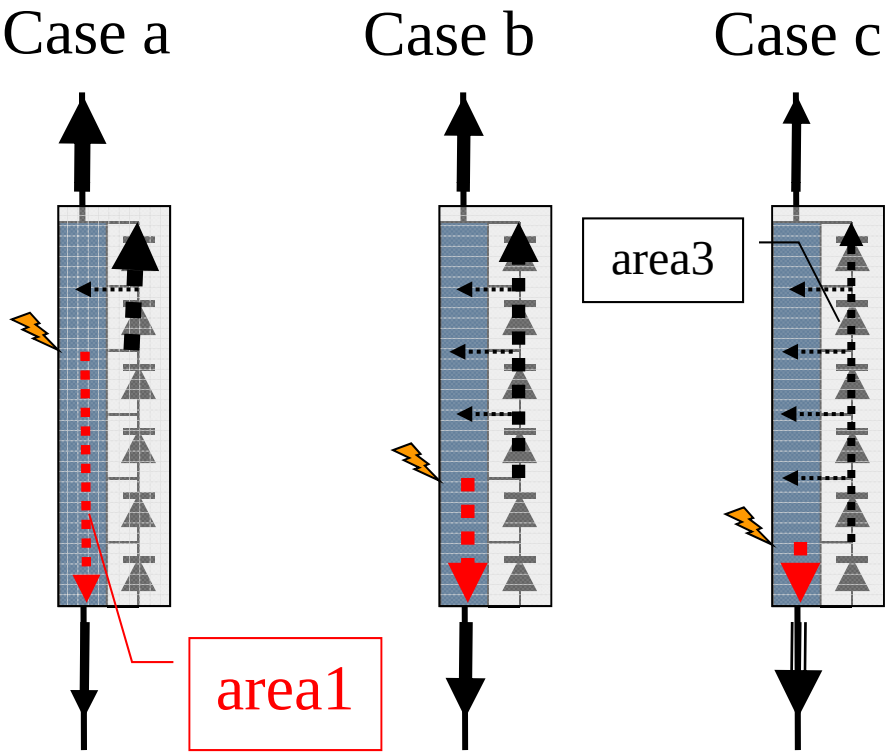
Flashover current distribution in ESD site circuit

The flashover current distribution in ESD site circuit is versus the ESD site location in this circuit

For case a, n is higher than 0.8 x Ns then the flashover current is flowing mainly by the top circuit.

For case b, the ratio Ifot/Ifob = 1.

For case c, n is lower than 0.2 x Ns then the flashover current is flowing mainly by the bottom circuit.



Current calculation simplification assumption

The current is composed by

- the steady state current due to the photovoltaic effect, about 0.5A (GaAs cell of 30 cm^2) per circuit,
- the transient current due to the ESD and flashover propagation ; this transient current in the ESD site is estimated in the range of 1 to 10 A versus the solar array panel size.

The first approach is to assume steady state circuit current 0.5A is negligible with regard to flashover current, because the GaAs cell operating point during flashover is

- either in cell reverse current mode, area 3
- or in cell reverse voltage mode, area1, (which is equivalent to bypass diode forward mode).

During flashover we assume the cell circuit flashover current is

- either in cell reverse current mode, area 3, so the operating voltage is quite Voc at cell level,
- or in cell reverse voltage mode, area 1, so the operating point current is higher to 0.5A.

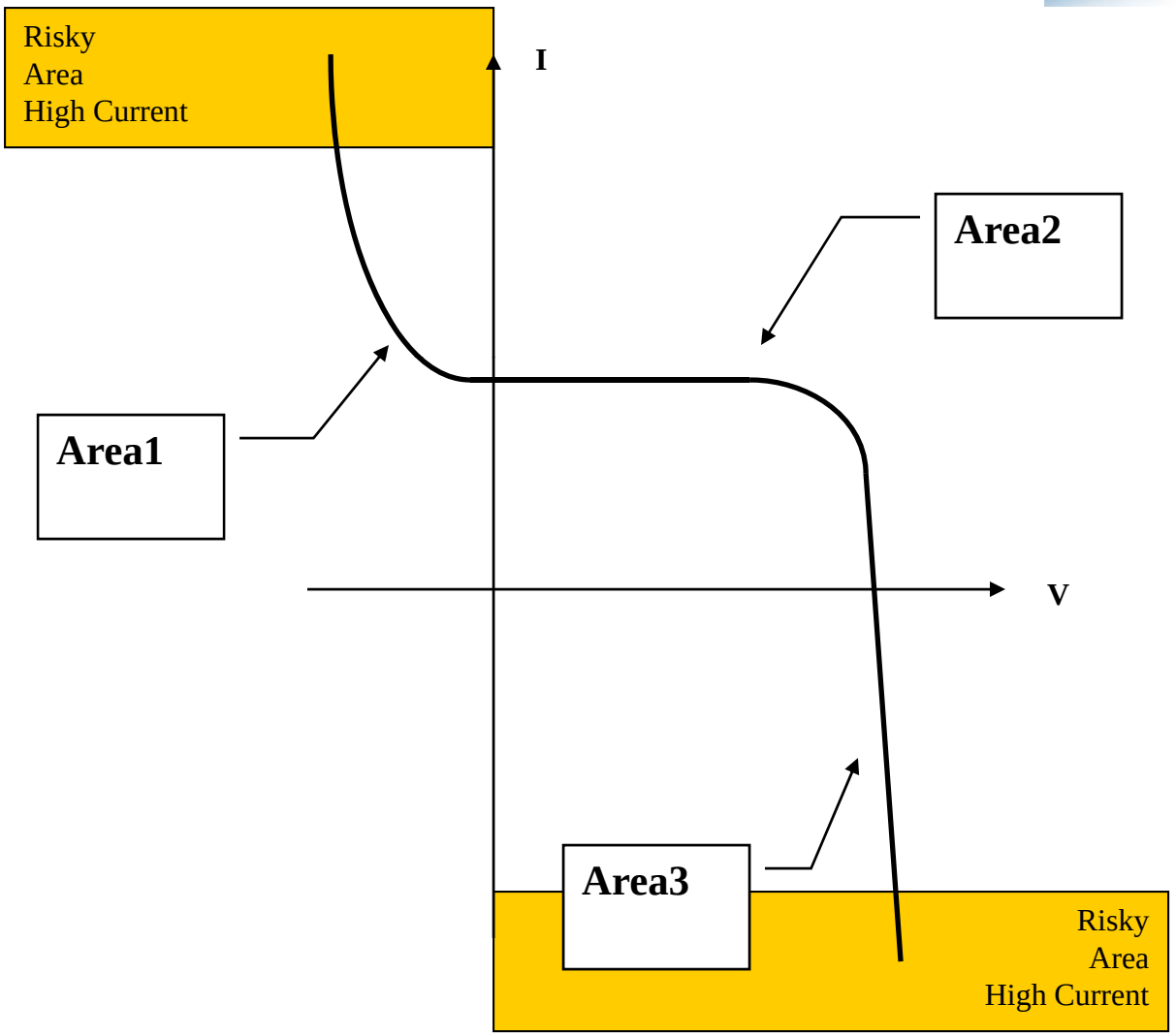
The current values are versus circuit architectures.

Identified risks

2 possible risks :

With high current

- **GaAs cell reverse current, area 3,**
- **bypass diode forward current, area 1.**



Architecture trade-off method

For each architecture case, we check the flashover current value

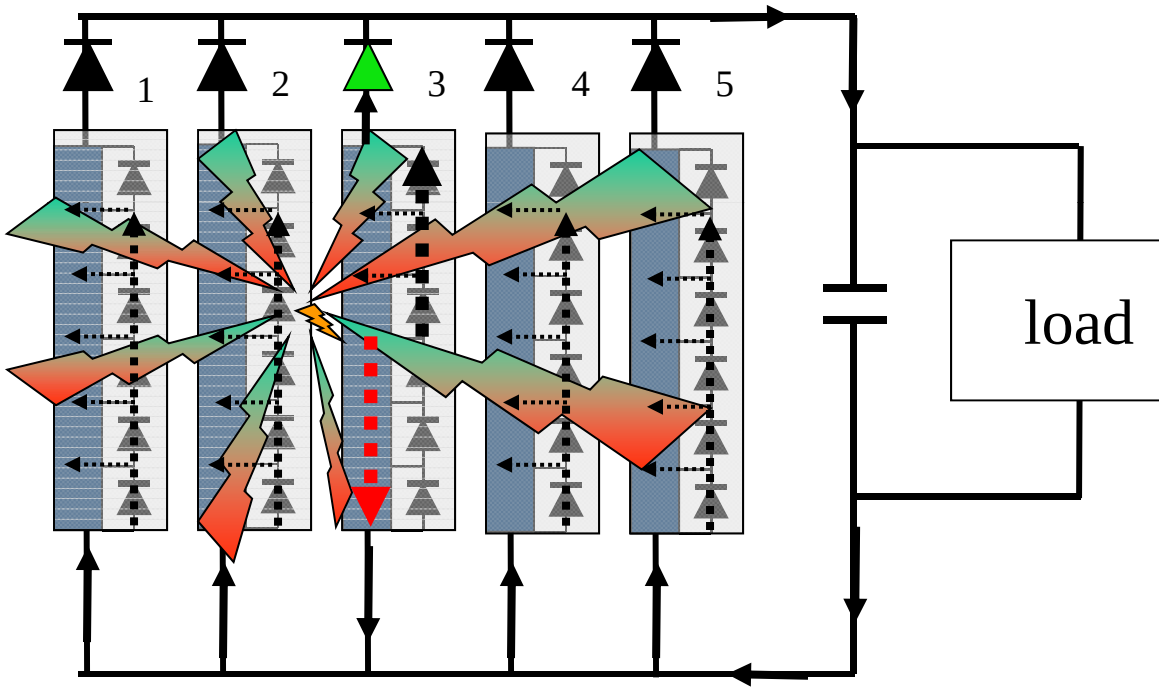
- for the both identified risks
  - GaAs cell reverse current mode, area 3,
  - bypass diode forward current mode, area 1.
- in each cell circuit type :
  - ESD site circuit
  - Other discharged circuit
- with the following scale
  - full flashover current : almost all current flowing in the ESD site,
  - part of full flashover current,
  - circuit flashover current : cumulated coverglass discharge current of only 1 cell circuit,
  - part of circuit flashover current,
  - no circuit flashover current.

Versus the ESD site location.

Architecture with blocking diode on the + top

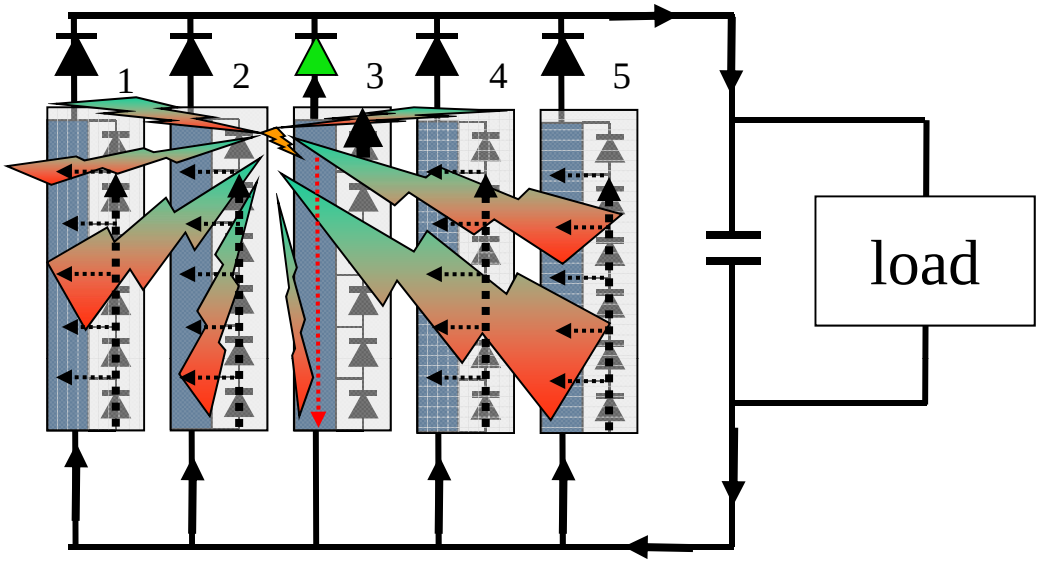
The ESD site circuit (n°3) current is flowing outside, by circuit top with forward current mode or by circuit bottom with cell reverse current mode.

The other discharged circuit (n°1-2-4-5) currents are flowing inside only by the circuit bottom due to blocking diodes (n°1-2-4-5) which are blocked.



Architecture 1 case a

n is higher than 0.8Ns then the flashover current is flowing mainly by the circuit top, by the bypass diodes. Bypass diode risk area is located on the circuit n°3 top with full flashover current.

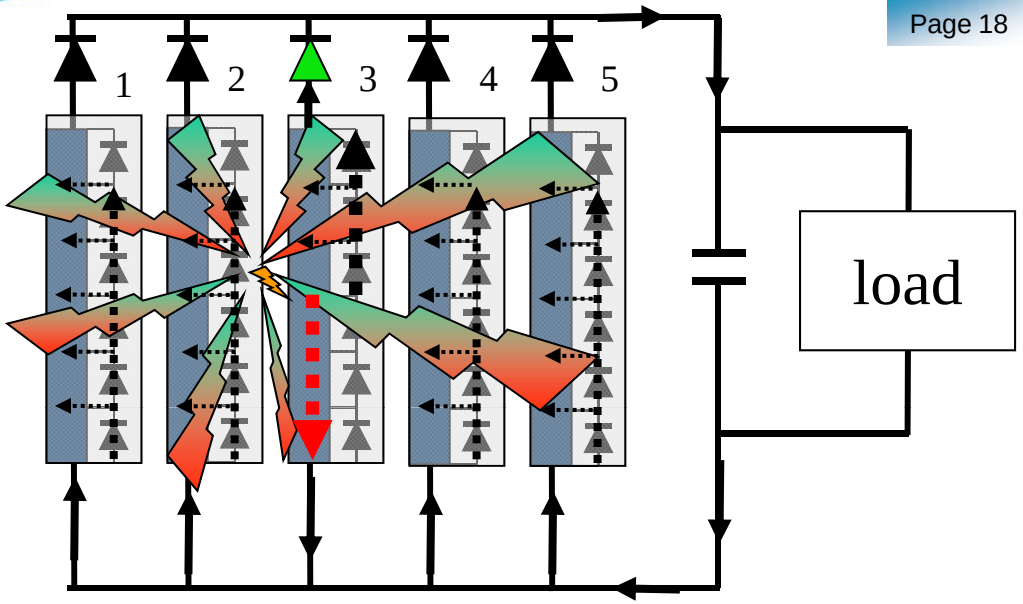


Architecture 1		Case a	Case b	Case c
GaAs cell reverse current mode	ESD site circuit	Part of circuit flashover current		
	Other discharged circuits	No Circuit flashover current		
Bypass diode forward current mode	ESD site Circuit	Full flashover current on top cells		
	Other discharged circuits	Circuit flashover current		

Architecture 1 case b

In the circuit n°3,

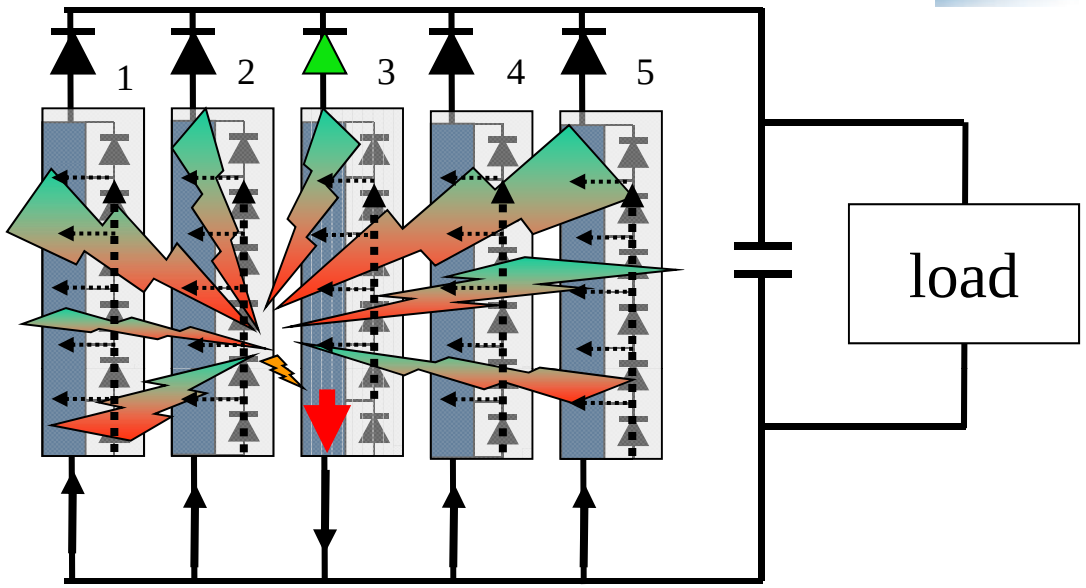
the ratio Ifot/Ifob is around 1



Architecture 1		Case a	Case b	Case c
GaAs cell reverse current mode	ESD site circuit	Part of circuit flashover current	Part of full flashover current on bottom cells	
	Other discharged circuits	No Circuit flashover current	No Circuit flashover current	
Bypass diode forward current mode	ESD site Circuit	Full flashover current on top cells	Part of full flashover on top cells	
	Other discharged circuits	Circuit flashover current	Circuit flashover current	

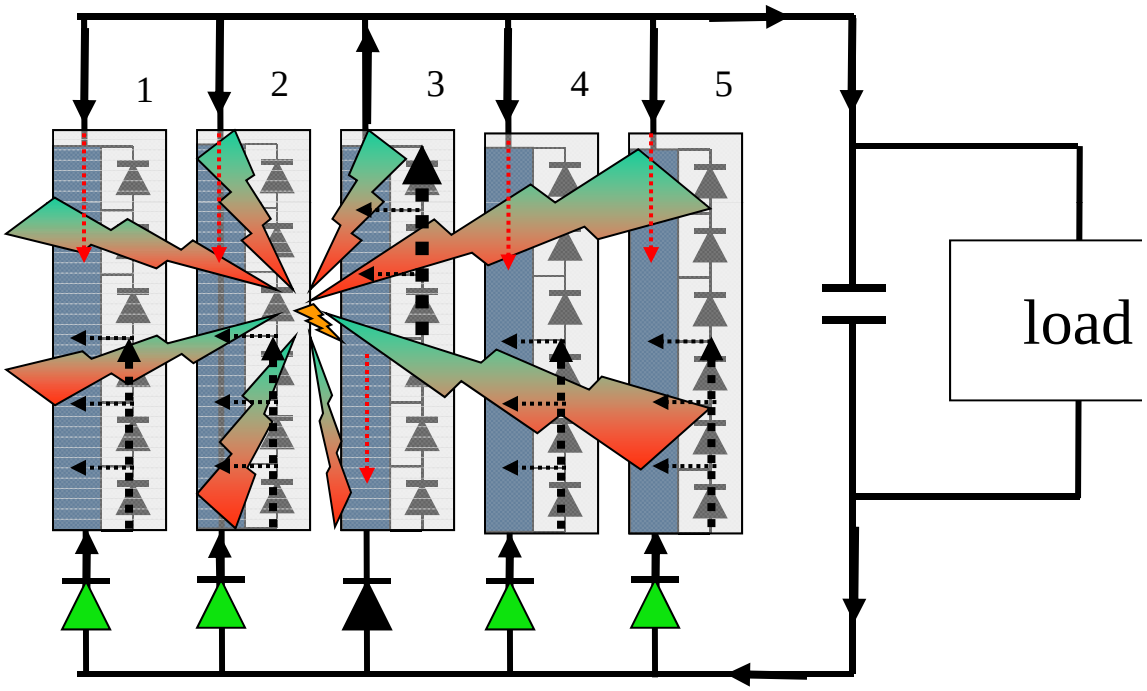
Architecture 1 case c

n is lower than 0.2Ns then the flashover current is flowing mainly by the circuit bottom , by GaAs cell in reverse current mode in the circuit n°3. GaAs cell risk area is located on the circuit n°3 bottom with full flashover current.



Architecture 1		Case a	Case b	Case c
GaAs cell reverse current mode	ESD site circuit	Part of circuit flashover current	Part of full flashover current on bottom cells	Full flashover current on bottom cells
	Other discharged circuits	No Circuit flashover current	No Circuit flashover current	No Circuit flashover current
Bypass diode forward current mode	ESD site Circuit	Full flashover current on top cells	Part of full flashover on top cells	Part of circuit flashover current
	Other discharged circuits	Circuit flashover current	Circuit flashover current	Circuit flashover current

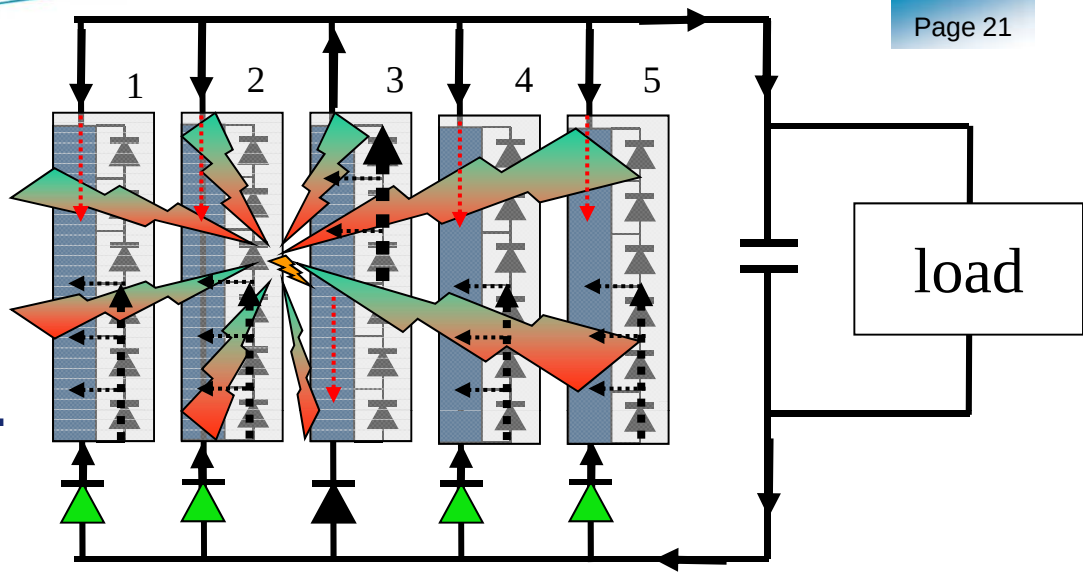
- The ESD site circuit (n°3) current is flowing outside only by circuit top with forward current due to blocking diode n°3, which is blocked.
- The other discharged circuit (n°1-2-4-5) currents are flowing inside , by circuit top with cell reverse current mode or by circuit bottom with forward current mode.



Architecture 2

For all case a, b,c, the flashover current is flowing only by the circuit n°3 top, by the bypass diodes. Bypass diode risk area is located on the circuit n°3 with full flashover current.

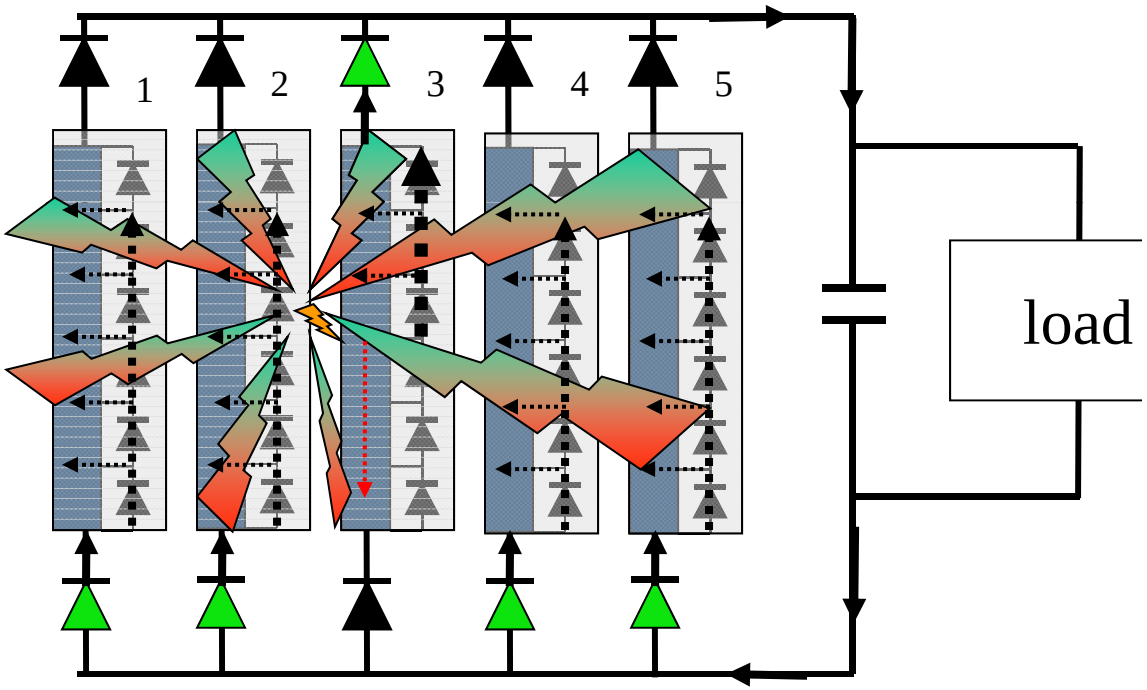
All circuit is with GaAs cell reverse mode risk but with only circuit flashover current instead of full one.



Architecture 2		Case a	Case b	Case c
GaAs cell reverse current mode	ESD site circuit	Circuit flashover current	Part of circuit flashover current on bottom cells	Few of circuit flashover current on bottom cells
	Other discharged circuits	Part of circuit flashover current	Part of circuit flashover current	Part of circuit flashover current
Bypass diode forward current mode	ESD site Circuit	Full flashover current on top cells	Full flashover current on top cells	Full flashover current
	Other discharged circuits	Part of circuit flashover current	Part of circuit flashover current	Part of circuit flashover current

The ESD site circuit (n°3) current is flowing outside only by circuit top with cell forward current due to bottom blocking diode n°3, which is blocked.

The other discharged circuit (n°1-2-4-5) currents are flowing inside , only by the by circuit bottom with cell reverse current mode, due to top blocking diodes n° 1-2-4-5, which are blocked .

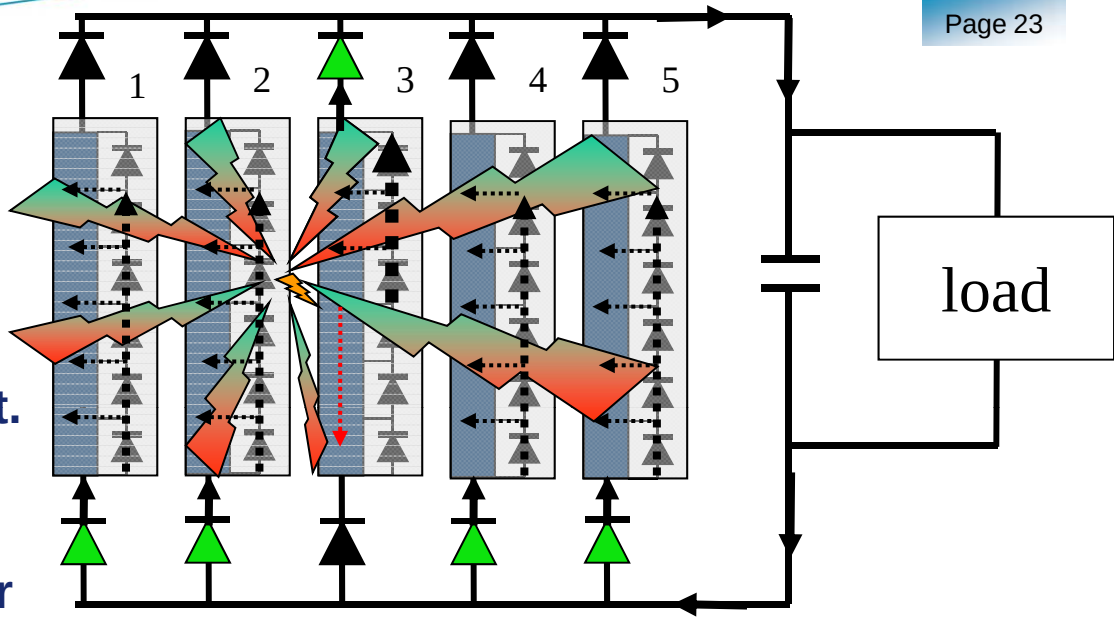


The flashover current is flowing in the top blocking diode n°3, solar array harness up to the power conditioning unit.

Architecture 3

For all case a, b,c, the flashover current is flowing only by the circuit n°3 top, by the bypass diodes. Bypass diode risk area is located on the circuit n°3 with full flashover current.

Only the ESD site circuit is with GaAs cell reverse mode risk but with only circuit flashover current instead of full one.



Architecture 3		Case a	Case b	Case c
GaAs cell reverse current mode	ESD site circuit	Circuit flashover current	Part of circuit flashover current on bottom cells	Few of circuit flashover current on bottom cells
	Other discharged circuits	No circuit flashover current	No circuit flashover current	No circuit flashover current
Bypass diode forward current mode	ESD site Circuit	Full flashover current on top cells	Full flashover current on top cells	Full flashover current
	Other discharged circuits	Circuit flashover current	Circuit flashover current	Circuit flashover current

GaAs cell reverse current mode (area 3)

GaAs cell reverse current mode	ESD site circuit	Case a	Case b	Case c
	Architecture 1	Part of circuit flashover current	Part of full flashover current on bottom cells	Full flashover current on bottom cells
	Architecture 2	Circuit flashover current	Part of circuit flashover current on bottom cells	Few of circuit flashover current on bottom cells
	Architecture 3	Circuit flashover current	Part of circuit flashover current on bottom cells	Few of circuit flashover current on bottom cells

- Architectures 2&3 are equivalent and better than architecture 1 for this case.

GaAs cell reverse current mode	Other discharged circuits	Case a	Case b	Case c
	Architecture 1	No Circuit flashover current	No Circuit flashover current	No Circuit flashover current
	Architecture 2	Part of circuit flashover current	Part of circuit flashover current	Part of circuit flashover current
	Architecture 3	No circuit flashover current	No circuit flashover current	No circuit flashover current

- Architecture 3 is better for this case.

Bypass diode forward current mode (area 1)

Bypass diode forward current mode	**ESD site circuit**	Case a	Case b	Case c
	Architecture 1	Full flashover current on top cells	Part of full flashover on top cells	Part of circuit flashover current
	Architecture 2	Full flashover current on top cells	Full flashover current on top cells	Full flashover current
	Architecture 3	Full flashover current on top cells	Full flashover current on top cells	Full flashover current

- This case is not discriminating, but shows high current for all architectures in the bypass diodes.

Bypass diode forward current mode	**Other discharged circuits**	Case a	Case b	Case c
	Architecture 1	Circuit flashover current	Circuit flashover current	Circuit flashover current
	Architecture 2	Part of circuit flashover current	Part of circuit flashover current	Part of circuit flashover current
	Architecture 3	Circuit flashover current	Circuit flashover current	Circuit flashover current

- This case is not relevant because higher current occur on ESD site circuit.

Architecture comparison conclusion

The more stressed cell circuit during ESD is the ESD site circuit.

During flashover propagation, the cell circuit number is not limited to 5 as described in the previous figures. The cell circuit number is lead by the flashover propagation. Flashover on (at least) 2 m² panel has been demonstrated , that means the number of circuits (except ESD site circuit, so called “other discharged circuits”) with partial flashover current may be high.

The probability for a cell circuit to be “other discharged circuits” type is higher than ESD site circuit.

These are why it is important to reduce flashover current in “other discharged circuits”.

Architecture comparison conclusion

The better reduction of risk of GaAs cell reverse current mode, area 3, is with architecture n°3, mainly for “other discharged circuits” type.

The risk of GaAs cell reverse current mode, area 3, is quite null if the duration is short.

Risk of bypass diode forward current mode, area 1,

- **On ESD site circuit, has no difference between the 3 architectures, with high current,**
- **On other discharged circuit has a slight difference which is without interest due to high current on ESD site circuit.**

This risk of bypass diode forward current mode, area 1, is null if the diode performance is at least 25A repetitive surge current, assuming that full flashover current is smaller than 15A.

Perspective & Acknowledgements

Perspective

- We need more experimental data about flashover phenomenon in order to estimate the flashover current and duration, versus solar array design.
- Versus these new experimental data about flashover, the risk of GaAs cell reverse current mode, area 3, and the risk of bypass diode forward current mode, area 1, may be updated. If necessary, solar array design may be modified.

Acknowledgements

- The work reported here was possible due to long discussions with solar array experts and ESD experts, in the world.

- A special thank to AZUR SPACE and SHARP Corp. that always provide various component data.